IN THE SPECIFICATION

Page 2, line 1, before "BACKGROUND OF THE INVENTION" please insert the following paragraphs:

--CROSS REFERENCE TO RELATED APPLICATION

This application claims the benefit and is a continuation of U.S. Patent Application No. 09/475,105, filed December 30, 1999 by Jonathan Douglas et al., now allowed.--

IN THE CLAIMS

Please cancel claims 1-36 without prejudice.

Please add new claims 37-42 as follows below.

1-36. (Cancelled)

37. (New) A pipelined instruction decoder for a multithread processor, the pipelined instruction decoder comprising:

an instruction decode pipeline to decode instructions associated with a plurality of instruction threads, the instruction decode pipeline having a predetermined number of pipe stages;

a valid bit pipeline in parallel with the instruction decode pipeline, the valid bit pipeline having the same predetermined number of pipe stages in parallel with the predetermined number of pipe stages of the instruction decode pipeline, the valid bit pipeline to associate a valid indicator at each pipe stage with each instruction being decoded in the instruction decode pipeline; and